layer formed in the device isolation insulating film and connected to the gate electrode, source and drain electrodes arranged on the substrate to face each other via the gate electrode, and an insulating film covering bottom and side surfaces of each of the gate electrode and the gate wiring layer, wherein the gate, source and drain electrodes and gate wiring layer have upper surface levels equal to or lower than that of the device isolation insulating film.--

IN THE CLAIMS:

Please amend claims 30, 31, 36, and 37 as follows:

30. (Amended) A semiconductor device comprising:

a substrate;

a device isolation insulating film formed on one major surface of said substrate,

a gate electrode formed on the major surface of said substrate;

a gate wiring layer formed in said device isolation insulating film and connected to said gate electrode;

a source electrode and drain electrode arranged on the major surface of said substrate to face each other via said gate electrode; and

an insulating film covering bottom and side surfaces of each of said gate electrode and said gate wiring layer; and

wherein said gate electrode, said gate wiring layer, said source electrode, and said drain electrode have upper surface levels equal to or lower than an upper surface level of said device isolation insulating film.

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31. (Amended) A device according to claim 30, further comprising a source diffusion layer and a drain diffusion layer below said source electrode and said drain electrode.

36. (Amended) A device according to claim 30, further comprising a connection wiring layer connected to at least one of said source electrode, said drain electrode, said gate electrode, and said gate wiring layer, said connection wiring layer having an upper surface level equal to or lower than the upper surface level of said device isolation insulating film.

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37. (Amended) A semiconductor device comprising:

a substrate;

a gate wiring layer formed on one major surface of said substrate;

an insulating film interposed between said substrate and said gate wiring layer and covering a side surface of said gate wiring layer;

a pair of thin films formed by epitaxial growing a semiconductor on one major surface of said substrate, and arranged on two sides of said gate wiring layer; and

a gate sidewall formed on said pair of thin films, covering said side surface of said gate wiring layer, and made of an insulator.

REMARKS

In this Amendment, Applicants amend the Abstract to comply with Examiner-required corrections, and submit a Request for Approval of Drawing Changes, also to comply with an Examiner-required correction. Applicants also amend claims 30, 31, 36, and 37 to more clearly describe the present invention. In accordance with the requirements of 37 C.F.R. § 1.121(c)(1),

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